UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,581	03/25/2004	Michael Karl Gschwind	AUS920030719US1	7129

45327 7590 01/18/2007

IBM CORPORATION (CS)
C/O CARR LLP
670 FOUNDERS SQUARE
900 JACKSON STREET
DALLAS, TX 75202

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,581	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-10,12-15,17,19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,12-15,17,19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 22 November 2006. Claims 1-5, 8-10,12-15,17,19, 21 and 22 are pending. Claims 6, 7, 11, 16, 18, 20 and 23-30 have been cancelled. All objections and rejections not repeated below are withdrawn.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 14 and 21 of U.S. Patent Application 10809579 contain every element of claims 1, 4, 12 and 13 of the instant application and as such provisionally anticipate claims 1, 4, 12 and 13 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 8-10, 12, 13, 15, 17, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson and Hennessy [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson").

Per claim 1, Patterson teaches a processing system, comprising:

a memory comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each having difference corresponding coherence directory data (Fig.8.22 and page 680, first paragraph, "a bit vector for each memory block");

a plurality of buffers interconnected to said memory (Fig 8.22, caches);

a plurality of processing elements (Fig 8.22, combination of processor and directory controller, see page 682, fourth paragraph), each said processing element interconnected to a different one of said plurality of buffers (see Fig 8.22);

wherein each of the processing elements comprises requesting means for requesting a selected one of said memory blocks from said memory (see Fig 8.24 and 8.25, and pages 682-685);

wherein the memory comprises means responsive to said requesting means for providing the selected memory block and the coherence directory data corresponding to the selected memory block to a requesting one of said processing elements (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph; and page 682, fourth paragraph, a processor requests memory for a write operation, the block is cached, its coherence directory value is tested to verify its 'exclusiveness', also see Fig 8.24 and 8.25, pages 683-685, 'write miss', volumes are sent to the owner processor, while the corresponding directory values are sent/written/updated to the directory. The

claims only stated that 'memory block' and 'coherence directory data' are sent to the processing element, but the claims did not state in what order they are sent); and

wherein each of the processing elements comprises means for receiving the selected memory block and the coherence directory corresponding to the selected memory block (see citation and notes set forth above), and for determining if the selected memory block is available for a particular access mode (page 682, fourth paragraph, "any cache block must be in the exclusive state when it is written and any shared block must be up to date in memory").

Per claim 2, Patterson further teaches the memory blocks are configured to provide a system memory (the distributed shared memory form the system memory space of the system shown in page 680, Fig.8.22, see Distributed Shared Memory Architecture, pages 677-685).

Per claim 3, Patterson further teaches the memory blocks are used to provide a level of cache in the system memory (memory blocks in cache/cache blocks, see page 679, paragraph 3).

Per claim 4, Patterson further teaches the processing elements are connected with the buffers via point to point links (each processor is connected to a cache via point to point link, see page 680, Fig.8.22).

Per claim 8, Patterson further teaches a request by a processing element for one of the memory blocks from the memory results in an updating of directory information to indicate a state requiring resolution (see the rejection of claim 12set forth below).

Per claim 9, Patterson further teaches the processing element issuing the request also issues protocol requests (see "Directory-Based Cache-Coherence Protocols", pages 679-685, the processing element includes the directory controller described in page 682, fourth paragraph, which issues directory coherence protocol requests).

Per claim 10, Patterson further teaches that another processing element detecting the state backs off and retries a request for the memory block at a later time ("exclusive state" on page 682, fourth paragraph and Fig 8.24 and 8.25 implies that when another processing element tries to access the exclusively owned block when it is being written to, it would need to back off and retry later until the block is no longer being written to; also, an uncached state indicates to other processors that the requested data is not present at the requested node, a Read Miss occurs; see page 684, lines 7-11 and pages 685, lines 1-3, also see Fig.8.25; coherence actions are performed to make the requested node the only sharing node, and other processors would retry the requests to the sharing node).

Per claim 12, Patterson teaches a method for providing memory data to a requestor of the memory data, the method comprising:

requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data (cache, memory and directory, see page 680, Fig.8.22);

generating a response including the memory data and corresponding coherence directory data (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph; and Fig 8.24-8.25, pages 683-685; also see claim 1's rejection as set forth above);

updating directory coherence data corresponding to the memory data (see Fig 8.25 and pages 682-685, during write, if the block is not in exclusive mode, a coherence/state change action is performed, also see rejection of claim 27 as set forth above),

receiving the response including the memory data and the corresponding coherence directory data from said memory hierarchy level (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph),

determining whether the received coherence directory data is compatible with a required access mode (see pages 682-685, see Fig 8.24 and 8.25 and the corresponding paragraphs explaining the figures; see page 682, fourth paragraph, "any cache block must be in the exclusive sate when it is written and any shared block must

be up to date in memory; the processing element is interpreted as the combination of Patterson's processor, cache and directory controller);

performing at least one coherence action if the received coherence directory data is incompatible with the required access mode (see fig 8.25 and pages 682-685, during write, if the block is not in exclusive mode, a coherence/state change action is performed),

providing the memory data to the requestor of memory data (see pages 682-685, also see "write miss" on page 685).

Per claim 13, Patterson further teaches requesting of the memory block, and the generating and receiving of the response, are performed by sending and receiving data over point to point links (the messages and replied data values are sent between the processors and the directories, with a single source and a single destination, hence point-to point links; see page 681, lines 5-16 and Fig. 8.23).

Per claim 15, Patterson further teaches that the coherence directory data is indicative of a state wherein at least one node is performing at least one coherence action as a result of receiving the response (state information provided under the columns "Processor", Coherence state of lock, and Bus/directory activity indicate the coherence actions are being performed with regard to directory information; see page 698, Fig.8.32).

Per claim 17, Patterson further teaches the at least one coherence action involves a processing element sending coherence request to another processing element (messages sent between processors, see page 681, paragraph 2, Fig.8.23 and page 682, last paragraph).

Per claim 21, Patterson further teaches the generating of the response is carried out under the control of a tag array (bit vector, page 680, lines 4-11).

Per claim 22, Patterson further teaches the updating of the coherence directory data involves the setting or resetting of a plurality of bits (bit vector values must be set and reset, see page 680, lines 4-11).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson and Hennessy [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson").

Per claim 5, Patterson further teaches at least one of the processing elements comprises at least one processor (see processors, page 680, Fig.8.22). Patterson does not specification teach that at least another one of the processing elements comprises at least two processors. However, it is clear that having at least two processors at one computing host increases computing performance and reliability as compared to having only one processor, and therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to have another of the processing elements to comprise at least two processors.

Per claim 14, Patterson further teaches the step of generating the response is performed atomically with respect to other generating and updating steps (see page 684, lines 3-5). Although Patterson does not specifically disclose that the step of updating the coherence directory data is also performed atomically, it does suggest it (some actions are atomic, see page 684, lines 3-5; implementing cache coherency using atomic operations, see page 695; paragraph to page 699). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to perform updating directory information atomically to avoid inconsistency in the shared data due to access conflicts and incoherency.

Per claim 19, Patterson further teaches the response comprising the memory data and the corresponding coherence directory data is transmitted separately (see page 682, last paragraph), not in a single response. However, it would have been

obvious to one ordinarily skilled in the art at the time of the Applicant's invention to send the two pieces of data in a single response to reduce network traffic overhead and increase network throughput, as two separate responses would require at least two packets instead of the minimal of one packet for a single response. The number of transactions would also be reduced. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to transmit the memory data and the corresponding coherence directory data in a single response for the advantages set forth above.

Response to Arguments

8. Applicant's arguments filed on 22 November 2006 regarding claims 1-5, 8-10,12-15,17,19, 21 and 22 have been considered but they are not persuasive. The claims are taught by Patterson as set forth above.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

12 January 2007

Reginald D. Bragdon
REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100